# Tuned reticle enhancements optimized for process response

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**ABSTRACT**

The International Technology Roadmap for Semiconductors' history details the growing complexity of device design and the latest device-manufacturer's techniques for tuning their process for each new design generation. In spite of the current desire to incorporate techniques termed 'Design for Manufacture' (DFM) into manufacturing, simulations and the design cycle, they do little more than optimize feature quality for ideal exposure conditions while testing for shorts, opens and overlay problems over process variations.

The manufacturing linkage method in DFM simulation is performed by the adaptation of a technique unchanged in the last 30 years – 'process window analysis'. With this methodology, recent successes seen in chip-design have not taken their share of the burden of technology advancement. The lack of adequate manufacturing awareness in designs, coupled with materials design problems for extreme ultraviolet (EUV) lithography technology, recently redirected industry's path into critical layer splitting, a technique termed 'double patterning'.

Design optimization by simulation focuses on feature layout optimization for resolution. Design solutions that take advantage of the full potential spectrum of mask-feature alternatives to increase the functional process space and to simplify setup in manufacturing do not exist since there is no method of feedback. A mechanism is needed that can quantify design performance robustness, with mask-contributions, to variations in the user's specific manufacturing process.

In this study, a Process Behavior Model methodology is presented for the analysis of feature profiles and films to derive the relative robustness of response to process variations for alternative optical proximity correction (OPC) designs. Analysis is performed without regard to the specific mechanics of the design itself. The design alternatives of each OPC feature are shown to be strong contributors not only to resolution and depth-of-focus but also to the stability of final image response; that is, the ability of the feature profile to remain at optimum under varying conditions of process exposure excursion.

A method of extracting the systematic component of each feature's design-iteration is derived, providing the ability to quantify the specific OPC response sensitivity to changes in the exposure and process films as well as drift introduced by the tools of the exposure set.

## Motivation and introduction

### Speed-bumps in the roadmap

After a decade of smooth transition down the technological roadmap provided by Moore's Law, the semiconductor industry encountered a speed-bump in 2006. The ITRS roadmap for 2005, in outlining the path to sub-65nm MPU half-pitch production, highlighted the need for 'litho-friendly design rules' as it coupled the path with some very complex process sequences needed to achieve these goals [1]. The plan smoothly transitioned down a well-known trail where design segments of our industry presented the need for improved simulation accuracy coupled with chip-designs that are optimized to the characteristics of production.

The 2005 technology roadmap predicted a bend in the road due to occur around the turn of the decade when a major transition to extreme ultraviolet (EUV) illumination would be implemented to assume the production burden of 45nm Flash devices. As tool development in 2006 progressed, so did the clarity of the road ahead. It could now be clearly seen that a mountain of basic materials problems had to be surmounted before a production capable toolset could achieve the major transition to EUV. The industry speed-bump arose while warnings of a short detour into double patterning, or DP (see Figure 1), promised to continue the industry along the trail while conveniently pushing the EUV transition another five years down the path.

DP is conceived as a way of extending the current proven immersion 193nm (i193) excimer laser lithography to smaller feature sizes by splitting the most complex layers of new designs into two to five imaging levels. Each split level requires sequential exposure and development of different resist films and multiple etch steps to transfer the pattern-mask into the substrate. Photomask manufacturers will not see any relief since as the levels are split, the complexity of each reticle is maintained at the most aggressive current levels. The intent of this technique is to allow the level of reticle enhancement to remain in stasis while continuing progress a few more nanometers (nm) down the trail.

The ultimate cost of DP, however, may be underestimated. Continued progress along this detour is not free. DP technology is accompanied by increased within-layer pattern-to-pattern registration demands to the mask-maker as well as the device manufacturer. The methodology presents a need for some very clever pattern-splitting algorithms in chip design to minimize the number of splits. The adaptation of this technique will add to the already high number of mask layers projected for production to levels beyond the 36 MPU levels envisioned in 2005 for 32nm half-pitch production. Furthermore, demands on process control will multiply with the additional need to control multiple reticle pattern shifts, rotation and effective critical feature sizes within a single device layer in the presence of whole-wafer process and exposure tool systematic drift whose errors are, for the first time, derived from both reticle and wafer fabrication steps.

Even more fundamental to the industry as a whole, DP promises to add two to five levels for maximum complexity designs with their associated processing to the device recipe for every 'split' layer. The burden on photomask fabrication arises not only from the addition of complex levels but a whole new chapter of demands for improved pattern and alignment mark registration.

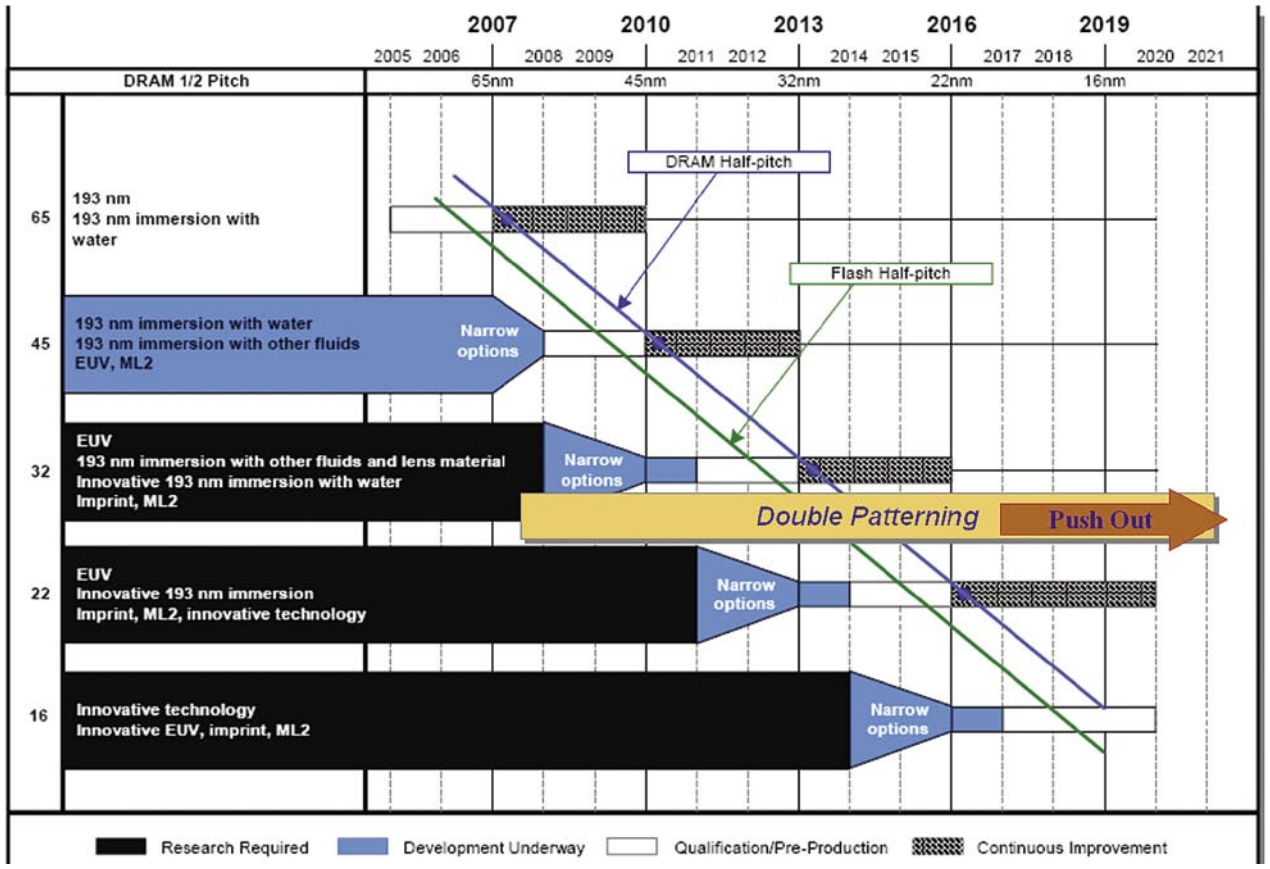


Figure 1. The ITRS 2005 roadmap insertion of a new 'double patterning' element to gain development time for EUV.

Fundamental library concepts for pattern and alignment features will have to be addressed because of the critical within-layer demands of pattern and alignment-mark registration. Base capacity in both photomask and wafer fabrication will be further lowered by the potential registration need to restrict production flow across dedicated exposure tools to reduce single-layer systematic errors.

DP has been introduced to gain time for EUV research largely because the industry did not meet this need by responding to the ITRS call for 'improved chip-designs optimized to the characteristics of production'. The detour into DP may be inevitable but economic considerations justify any approach that can push out the onset of production down this pathway. One solution lies in the extra process advantage to be gained through a closer link between the design and device production segments of the industry. This solution must incorporate an approach that truly extends the utility of the Design for Manufacture (DFM) concept by allowing final mask tape-out to be easily optimized to the characteristics of the individual wafer-fab and ultimately the individual lithography cell.

## Current problems in litho-friendly design

The current approach to litho-friendly designs involves extensive use of process simulation that employs fundamental photoresist and wavefront models to predict the final imaging of mask structures. Complex masks used for critical levels incorporate non-printing, sub-resolution patterns or phase shifting features to enhance imaging of the most critical image areas associated with low contrast, often called 'low $k_1$', feature elements. These non-printing active structures act as optical elements to locally modify the wavefront, forcing it to print the high-density, proximity sensitive features of today's devices [2].

Simulations historically focused only on the few, critical features of a layer for initial process setup. Software-based wavefront simulation, even in this restricted application, involves lengthy simulation times. A recurring problem with the limited scope of such simulations has been the occasional appearance of defect-prone pattern 'hot-spots,' where the non-printing mask elements are imaged or a disappearance of feature elements occurs during the normal excursions of the manufacturing process about the ideal exposure point.

Design for Manufacturing (DFM) has been pursued as a solution that couples these lengthy simulations to greater areas of the device-layer design in search of these 'hot-spots.' The resulting need for speed has driven the technology from software-only applications to specially designed parallel-processing computer hardware capable of calculating feature imaging for the entire layer [3]. As a DFM solution, the only manufacturing-specific linkage that these advanced simulators present to 'lithography aware design' involves the investigation of the measured 'process window' of the target process to estimate the production boundaries of focus and dose. This link results in a 'hot spot' simulation that primarily calculates the probability of shorts or opens in the final printed image but also addresses the potential for CD size variation, line-end pullback and the inclusion of 'extra patterns' from printing of sub-resolution enhancement features [4]. The analysis does nothing to expand the tolerance of the design to localized exposure variations in the process that would simplify manufacturing and increase the yield of higher performance devices.

The DFM-process window link has existed in its present form for over three decades [5]. Calculations – historically used to estimate initial focus and dose for setup – are now applied as the defining tool of exposure excursions in manufacturing. This is an application for which the technique was never designed and for which it is certainly not optimized.

Simulators enhance chip-design performance by analyzing pattern layout for the fidelity of feature replication at optimum exposure. Simulations do not incorporate an analysis of the manufacturing-process perturbation response to the many alternatives of each feature's reticle enhancement technology (RET) design. Yet, the implementation of this analysis would not only result in more robust lithographic performance but would also drive a concurrent reduction in the complexity of tool setup and process control.

Most process controls neglect the photomask as one of the largest sources of across-chip line-width variation (ACLV). When considered, the mask contribution is assumed stable throughout the process window ignoring the reality that it incorporates both static perturbation signatures, due to feature size offsets, as well as dynamic, optics, process and film sensitive signatures that vary with exposure as well as the unique aberrations of the exposure tool [6].

Limited progress has been made using simulations calibrated to a specific user's process. These calibrations do not incorporate the full-field process-space response of feature alternatives but rather rely on simulations to inject generic perturbations to calculate wavefront interactions. The method neglects the convolution of systematic manufacturing perturbations with the mask-process induced dynamic response of the photomask 'lens elements.'

DFM techniques therefore do not take into consideration the highly significant manufacturing conditions that vary continually during production such as the interaction of toolsets, process recipes and the incidence of process-induced reticle haze. The complex response of aerial image interactions with the translucent wafer film-stack presents a quantifiable influence that is strongly subject to the final design of the RET structure.

A small level of improvement in the mask design can be achieved through inverse lithography simulation but even here a lack of significant process-response linkage limits these interactions. Even here, the number of design alternatives presented by simulation is not systematically evaluated for optimum performance in the manufacturing facility.

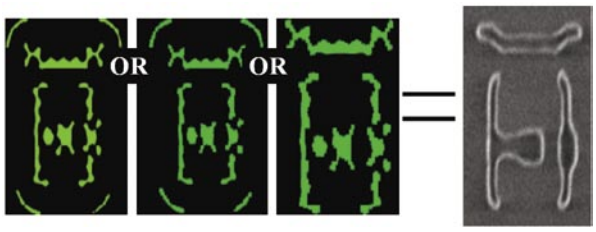


Figure 2. Three design alternatives for an SRAM gate binary mask pattern. Design, simulation and wafer.

Image courtesy of Luminescent Technologies (http://www.Luminescent.com)

The industry needs a methodology that not only optimizes device-image fidelity for ideal processing conditions but can also expand the process awareness of the sequence to select mask-design alternatives that improve manufacturability.

## DFM solution by process behavioral model characterization

Sub-resolution enhancement features, often called 'serifs', do not print under optimum exposure conditions and yet they continue to perturb the behavior of the final image. Many paths are available when serif design alternatives are considered. The primary reason for simulation of the photoresist image, given reticle pattern layouts, is the fact that 'what you see' is NOT 'what you get.'

Inverse Lithography Technology (ILT) provides an easily visualized example of the alternatives available to chip design. Unlike classic simulations, ILT begins with the desired final image on the wafer and simulates the ray-trace back through the optical system of the scanner in reverse order. For 'low $k_1$' applications, this results in patterns that only vaguely resemble their final image on the wafer as shown in Figure 2. At the optimum exposure, any of these mask-patterns will result in the desired wafer image, however, the overall image response of each across the process-space will differ significantly.

Pre-tapeout design alternatives therefore provide an opportunity to optimize the process performance of each class of mask pattern and establish a customized set of response guidelines for the end process. The design-alternative response surface can be algorithmically defined for each unique process and can then be applied to each new mask design for process-performance optimization.

We next present an example of a model-driven method of analysis of photoresist profiles derived for several OPC mask-design alternatives. This method characterizes a design's process response without having to consider the specific mechanics of the design itself. Each OPC feature is shown to be a strong contributor not only to resolution and across-chip line-width variation (ACLV), but also to the stability of final image response across an extended process exposure space.

Several different OPC designs for 70nm features at half-pitch, 1:2 and 1:3 periodic loading (see Table 1) are compared for their response stability to fluctuations of the process and the exposure tool perturbation set. A new concept in Process Behavioral Models is next presented to provide the extraction of the systematic interactions of each design with the normal fluctuations of the process space with those introduced by the toolset and film-stack.

With this approach individual feature design alternatives can be comparatively characterized to derive a systematic response surface representing all design options. Application of the response

TABLE 1. PATTERN DESIGNS AND CHARACTERISTICS. V = VERTICAL PATTERN EDGES, H = HORIZONTAL.

| Design | Orientation | Loading |
|---|---|---|
| 24B2<br>54A | V&H | 1:1 |
| 46E4<br>50G4 | V&H | 1:2 |
| 74E6<br>38F7 | V&H | 1:3 |

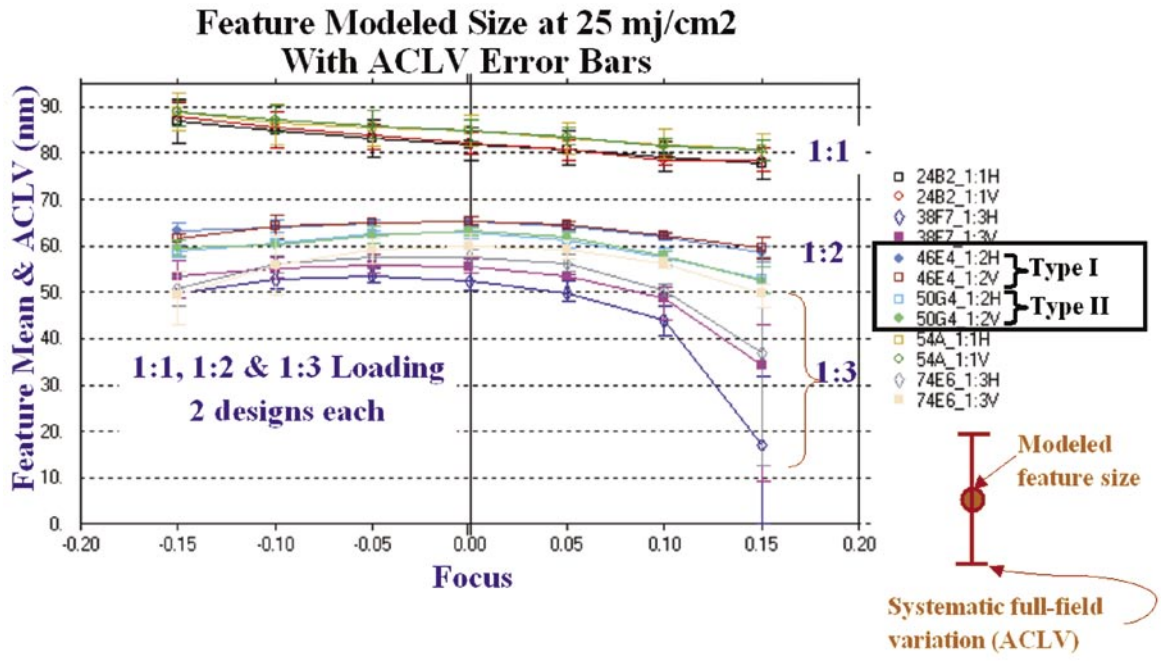


Figure 3. OPC family response to focus with ACLV sensitivity error bars at optimum dose. The results are produced using TEA Systems' Weir PW commercial software.

algorithm to any new product design ultimately provides the final reticle-design set that optimizes imaging for maximized manufacturability. Unlike simulation techniques, this method provides a customized analysis that considers the end-process's full process-space plus the contributions from the unique toolset and film-stack variance.

This method reduces the process-induced spread of feature variation about the design target and results in higher yields of high-performance final circuits. The resulting mask set will therefore also simplify exposure-tool and process setup for each unique product design.

## Process Behavioral Model formalization

At this point the classic process window algorithms of Bossung are left behind in favor of a set of models that consider both exposure and process perturbations of the process space. It has been shown that process disturbances are predominantly systematic in nature and can be described through a relation of the form equation 1 [3] (see below), where $FR_a$ is the feature response for pattern structure 'a' that is the product of a series of process disturbances 'm' and their sensitivity coefficients $\Lambda_a$. The 'feature response' in this application can be any metrology profile or film feature.

For this discussion we will define exposure as the local focus and energy applied to the image field and the dose will refer to the energy imparted to the exposure. The spatial response of the pattern can therefore be described as equation 2 (see below).

Equation 2 describes the perturbations across the field as a function of the radial and angular ($\theta$) position on a given exposure (F,D). Cylindrical coordinates are used in this example but other models can be substituted for a scanner-optimized response. The residuals to equation 2, embodied in $R_a$, will contain a small set of wafer contributed systematic errors as well as the random errors of the data.

We define the model set describing feature performance for a given feature design as the set of Process Behavioral Models or more simply its 'Process Response.' Using this model, the base response of any feature design to a given set of exposure conditions can be quantitatively described by the offset coefficient $\beta_0$. The corresponding sensitivity of the design's interactive sensitivity to image aberrations and mask perturbations is embodied in the systematically summed coefficients 1 to *n*.

The offset coefficient follows the classic Bossung response to defocus and dose. Derivation of the optimal process window elements of depth-of-focus (DoF) and exposure latitude (EL%) from this point onward is straightforward. Simultaneously, a feature design that minimizes the impact of higher order elements of equation 2 will result in a process response with greater DoF and EL% that simplifies the control and setup of semiconductor production and increases overall device yield.

## Measuring overall design robustness

The perturbation models of equation 2 have been applied and then, extending the offset coefficients to a Bossung analysis, we generate the first descriptive analysis of feature response in Figure 3. At first glance this appears to be a classic Bossung defocus graph but the information contained here is more representative of device response than a simple plot against focus would embody. By modeling the data, the analysis has

$$FR_a = \Lambda_a \star D_m$$

Equation 1.

$$FR_a(r,\theta) = \beta_o + \sum_{j=1}^{n} \beta_j * r^j * (\cos(j\theta) * \sin(j\theta)) + R_a$$

Equation 2.

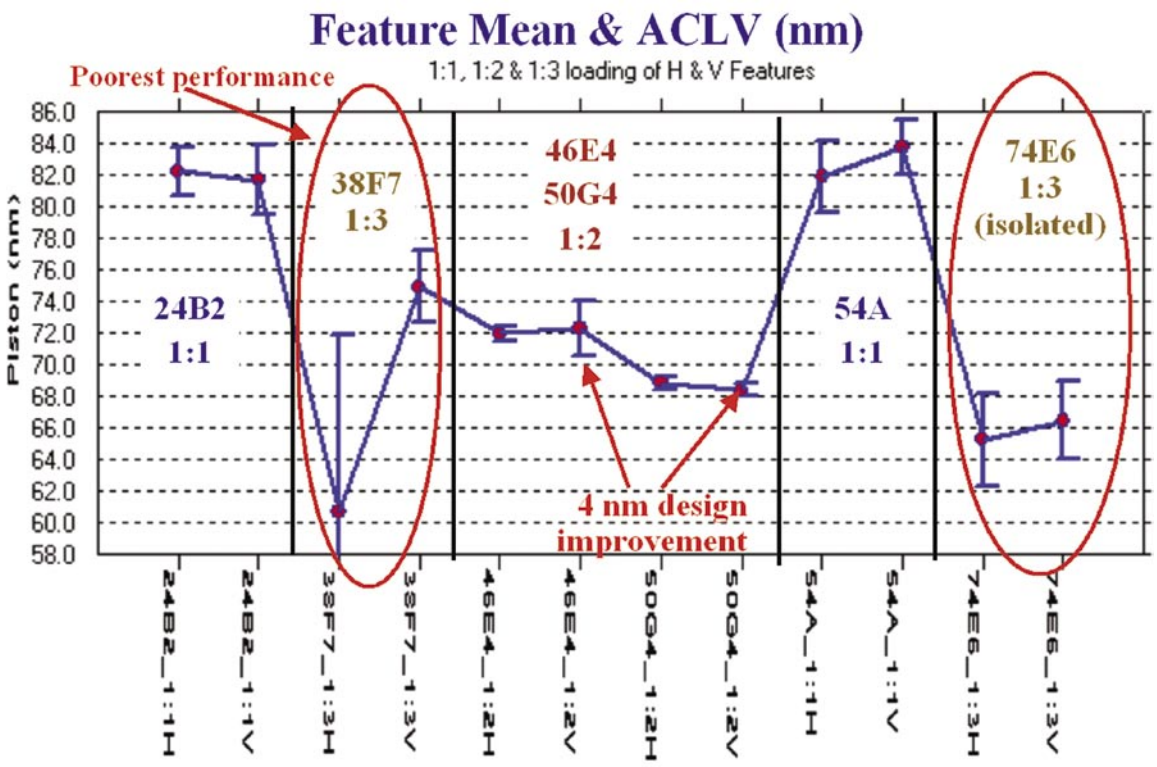


Figure 4. Full process space performance of four designs with modeled size and ACLV for the process-space.

eliminated the random metrology and exposure noise contribution and can directly measure the sensitivity of the feature-design aberrational response at each process-exposure.

Each data point plotted in the graph of Figure 3 represents the modeled full-field feature response for the exposure. The error bars of the data point detail the exposure's systematic ACLV yielded by the structure design. Our confidence level for reading a true feature response is greater with this method because the modeling process enables the accurate removal of soft errors embedded in the data by the metrology as well as the stochastic perturbations of the process.

All of the features presented in Figure 3 were targeted for a 70nm final size on the wafer. The chart as shown illustrates the now obvious design offset of the dense-packed 1:1 features from those of the 1:2 and 1:3 groupings. The 25mJ/cm$^2$ dose used to generate the data results in oversize 1:1 and undersized 1:2 and 1:3 loaded structures. However, there are additional artifacts that were not obvious to the original device designer in the form of inherent response offsets between the natural feature sizes for the 1:2 and essentially isolated 1:3 loaded features. Even more significantly, ACLV, shown by the error bars, varies significantly for the 1:3 data points where it appears to drastically rise out of control starting at 0.1µm defocus. This illustrates a significantly smaller operational process space than was suggested by any associated process window analysis.

Figure 3 also illustrates the near-isofocal response of the 1:2 feature set contrasted against the four 1:3 period feature designs that quickly deviate and fall-off in size above 0.1µm defocus (38F7). The basic 1:1 feature design is continually changing with focus suggesting a pattern density and size that may be beyond the capabilities of this process and exposure tool set.

One final characteristic of the base design shows a well-defined 3–4nm offset in response size between the vertically and horizontally oriented features for the 1:1 and 1:2 loaded features. This is an artifact of the averaging of the lens-slit aberrations that are present in only one scan-oriented-edge set of the feature. Proper feature-design selection is able to remove this offset resulting in a 4nm improvement in overall feature response.

## Feature-set response to the process space

A comparison of the feature-design response across the full process-space perturbation spectrum of this manufacturing step is shown in Figure 4. The response here exhibits the natural values attained by each feature-design and its associated range of systematic variation across the field and for all exposure conditions.

The 1:3 loaded feature sets exhibit the greatest variation in both the natural feature offset and their associated range due to process variations and aberration response. The strong 14nm performance offset between vertical and horizontal features for the 38F7 design is totally unacceptable as is the horizontal feature ACLV range. Comparing performance between these two '38F7' features, their ACLV range and offset, and the fact that the vertical feature size more closely follows the 1:2 loaded features, we must conclude that the horizontal feature design is at fault. The 74E6 designs, on the right side of the chart, are performing equally well with ranges in variation of about 5nm total and a 1nm difference in size between feature-edge orientations (V&H).

The best performance for this process, and the potential response for all feature loading, is presented by the 50G4 and 46E4 designs for 1:2 loading. A 3nm offset between these designs' base response illustrates that the nominal feature size can be more closely adjusted at the design phase. The vertical features of the 46E4 design exhibit about 3nm more ACLV than that of the horizontal ones, illustrating a sensitivity of the design to reticle scan direction.

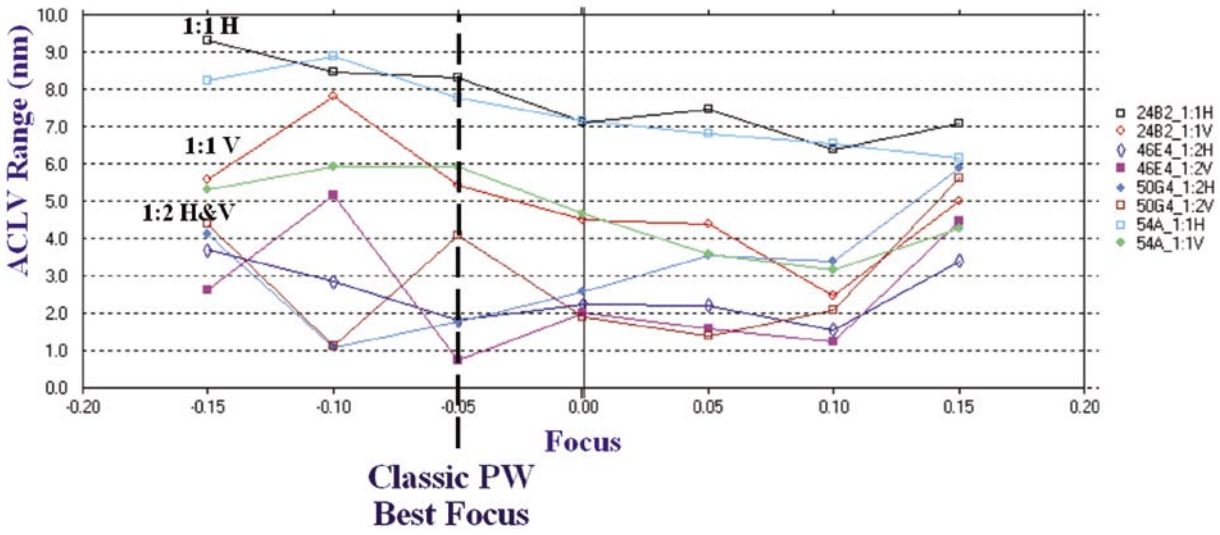


**Figure 5. ACLV design response at 25mJ/cm² for varying defocus of 1:1 and 1:2 loaded 70nm features. Classic techniques suggest optimum focus to be located at –0.05µm but ACLV is minimized if +0.05µm is used.**

A design engineer employing the structures used in this experiment would therefore select the 50G4 design specifics for 1:2 feature loading along with the 1:3 features generated by the 74E6 structure that just marginally meet the ACLV specifications set out by the ITRS roadmap. A representative sampling of enhancement feature alternatives, subject to the design constraints of each feature family, can then be used to systematically determine the pattern options that would provide even greater process stability for the final device reticle.

## Asymmetric ACLV dose response

Feature uniformity across the exposure field changes as the feature-design attempts to compensate for changing dose and non-optimum focus conditions. These changes are highly systematic and can be tuned for minimization by proper RET design. The modeled ACLV ranges for a set of 1:1 and 1:2 loaded features are shown in Figure 5.

We next examine the detailed ACLV focus response of the 1:1 and 1:2 loading designs using the graph of Figure 5. A classic process window analysis of this feature set calculated an optimal defocus setting of –0.05µm. Figure 5 shows a well-defined sensitivity to scan or slit direction in the 1:1, 70nm feature designs with a reduction in ACLV as defocus is moved from the process window 'optimum' of –0.05µm up toward +0.1µm.

The 1:1 loading designs also exhibit a 3nm ACLV increase with features oriented with their edges parallel to the direction of the slit (horizontal features) suggesting a stronger sensitivity to reticle scan direction. The 1:2 loaded features show this sensitivity only when defocus is greater than zero and then the ACLV increase is only 1nm.

Operational ACLV could be minimized by setting nominal production defocus to approximately +0.05µm as opposed to the –0.05µm suggested by the classic process window analysis. A design analysis also suggests that the 46E4 design for 1:2 loaded features performs better than the other options for response uniformity.

## Formalization of design response for specific processes

Simple examples of the layout alternatives in reticle-object design that can be applied to a binary photomask to obtain a final wafer image were shown in Figure 1. Inverse lithography (ILT) binary and optical proximity correction (OPC) reticle enhancement technology masks contain feature optimization types that can be broken into response families such as:

1. Feature density or period
2. Neighbor proximity
3. Line-end shortening
4. Vias
5. Substrate variations such as conductor or active area crossovers.

Reticles with phase-shifting structures rely on variations in etch-depth, undercut, phase-shift-area and other 'family-descriptive' response artifacts that can also be classified in this manner.

Each family-type generates a spectrum of wavefront signatures that will remain stable when created by a specific reticle-manufacturing process and applied in a specific wafer production environment. Even greater improvements can be achieved if the mask is specifically tuned to the matched set of aberrations found in a single photolithographic cell.

As an example, the serifs that define the final shape of the high-frequency components of a low contrast image can be employed with varying shape and distance from the printing feature. Variations in the subset of serifs that will define a satisfactory image will include serifs whose shape, separation and size can be systematically altered over a contiguous space bounded by the design constraints. A test reticle created with representative serif settings is then used to characterize the target semiconductor process.

Results derived from a single focus-dose matrix analysis of this test reticle for each family's process response are then used to generate a formalized process response surface for the technology family. This algorithm that now represents the systematic production response of ACLV behavior can then be used to optimize each family's process-manufacturability and lithographic yield while considering placement anywhere on the exposure field.

Any device-design employing this family algorithm will then be pre-optimized for the target combination of mask and wafer processes. Device alternatives are applied during the tapeout portion of the design cycle and are uniquely applicable to the target mask-and-wafer process.

The resulting mask set is a process-tuned reticle design that is not only free of 'hot-spot' sensitivities but optimized to provide an expanded process-space tolerance that both simplifies production control and yield.

## Conclusions

The current 'Design for Manufacture' approach of the industry is very complex. Photomask file-sizes and workloads spiral while users attempt to conjure imaging schemes that favor specific feature designs without systematic feedback representing performance. The eventual adoption of a double patterning solution to proximity problems only promises to temporarily stall the complexity trend spiral while simultaneously increasing photomask and process control burdens.

Simulators used for mask pattern design currently drive toward the resolution of the features with little regard for process-space response and stability. Even the incorporation of classic process-window links in the simulation does little more than search for shorts, opens and gross feature-size variations. Process tolerance of the design and the unique capabilities of the device manufacturer are not considered attributes during simulation.

A simpler and more cost effective approach to optimized design selection has been presented in techniques that can compare the performance of critical-feature design alternatives and model their robustness to a user's unique capabilities. This ability to generate process and design-specific Process Behavioral Models provides the opportunity to evaluate the full spectrum of design alternatives, photomask-manufacturing signatures and device-manufacture process capabilities to select an optimum set of patterns from the basic design alternatives of the reticle. The result is a photomask that works best for each target process and exhibits superior tolerance to process variations while minimizing the hassle involved in the complex techniques currently used to control illumination characteristics on the exposure tool.

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